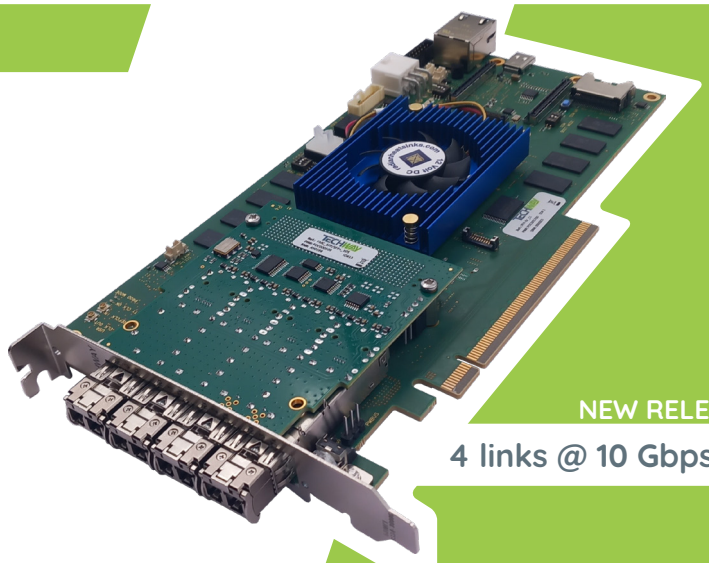
RAVEN

sFPDP PCIe PLATFORM

TECHWAY
SIGNAL VISION SYSTEM

Ready-to-use & cost-effective platform



NEW RELEASE
4 links @ 10 Gbps

APPLICATIONS

- RADAR
- SONAR
- Electronic Warfare
- Medical imaging
- Infrared imaging system
- Range & Telemetry system
- Physics research
- Video production

BENEFITS

- COTS sFPDP platform
- VITA 17.1 & VITA 17.3 compliant
- Optical or/and copper SFP modules
- Multi-board application support
- Low power
- Windows & Linux compliant SDK

KEY FEATURES

- 4 sFPDP channels
- Up to 10 Gbps per link
- RAVEN-1 & RAVEN-3
  - PCIe x4 Gen2
  - AMD Kintex 7 FPGA
- RAVEN-3_2
  - PCIe x16 Gen3
  - AMD Kintex UltraScale+ FPGA
- Trigger input
- 8 User I/Os connector
- Independent clock per channel

DEFENCE

INDUSTRY

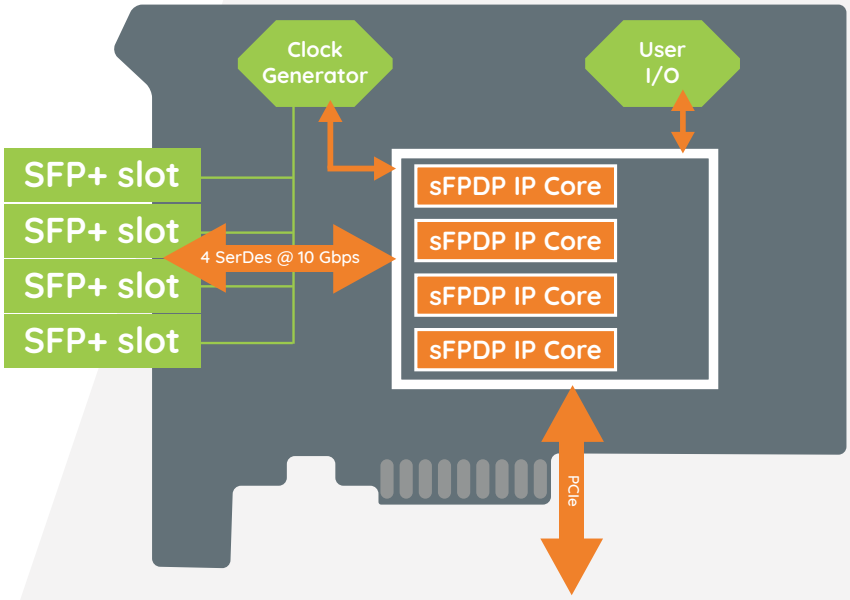
Serial Front Panel Data Port is a high-speed low-latency serial communications protocol for use in high-speed data transfer applications.

RAVEN is a flexible platform implementing 4 sFPDP channels with receive and transmit engine for high-performance data-processing.

Based on AMD (Xilinx) FPGA, this sFPDP platform supports up to 10 Gbps data rate per link. RAVEN is fully dimensioned to implement VITA 17.1 and VITA 17.3 sFPDP standards and offers the following functionalities : Flow Control, CRC, Framed/Unframed, Copy/Loop Mode.

The user-friendly API (Application Programming Interface) software, written in C++, allows to get/send data, monitoring, configure, upgrade, etc.

This platform is compliant with copper or fiber thanks to its SFP+ slots.



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SOFTWARE

- Linux (64 bits) supported
- Windows 10 & 11 (64 bits) supported
- Easy-to-use API
- Multi-board management
- Concurrent access supported
- SDK with example designs

ENVIRONMENTAL INFORMATION

- Operating temperature range : 0°C to 50°C
- Storage temperature range : -55°C to 125°C
- Maximum shock range : 10g during 20ms
- Maximum vibration range : 0.03 g2/Hz
- Compliant with RoHS process

ORDERING INFORMATION

- **RAVEN-1**
  - VITA 17.1 sFPDP platform, 4 channels, PCIe x4 Gen2
- **RAVEN-3**
  - VITA 17.3 sFPDP platform, 4 channels up to 10Gbps, PCIe x4 Gen2
- **RAVEN-3_2**
  - VITA 17.3 sFPDP platform, 4 channels up to 10Gbps per link, PCIe x16 Gen3

RAVEN product line is delivered as a ready-to-use platform. Its FPGA design is open to customization for specifics projects (on demand).

- **RAVEN_850_SFP_pack**
  - Set of 4x SFP+ transceivers multimode 850nm for RAVEN platforms
- **RAVEN_1350_SFP_pack**
  - Set of 4x SFP+ transceivers multimode 1350nm for RAVEN platforms

SOFTWARE DEVELOPMENT KIT

The RAVEN includes dedicated software packages. This board allows to manage up to 4 independent full duplex channels compliant with sFPDP protocol.

The SDK includes both C++ API and drivers to send and receive sFPDP data packets, according to sFPDP specifications.

Save development time with SDK features :

- Simultaneous sFPDP frame grabber and transmitter up to 4 channels
- Software frame buffer management
- sFPDP read back functionalities based on timestamp
- Board settings and configuration
- Statistics

An example design is provided to help developers to get familiar easily with the RAVEN SDK.

```
*** RAVEN System information ***
TwRAVEN API version: 1.0
TwPCIe Version     : 3.16
Design version     : 1.3
Design timestamp   : 20220202 / 105256
Design status      : 0x13

VITA standard      : 17.1
Data rate          : 2.49996 Gb/s

*** sFPDP Channel status ***
|------ CHANNEL 0 -------|------ CHANNEL 1 -------|------ CHANNEL 2 -------|------ CHANNEL 3 -------|

|-- SFP+                |-- SFP+                |-- SFP+                |-- SFP+                |
|TX Disabled         : o |TX Disabled         : o |TX Disabled         : o |TX Disabled         : o |
|TX Fault            : o |TX Fault            : o |TX Fault            : o |TX Fault            : o |
|RX LOS              : o |RX LOS              : o |RX LOS              : o |RX LOS              : o |

|-- sFPDP TX            |-- sFPDP TX            |-- sFPDP TX            |-- sFPDP TX            |
|TX Lane is Enabled  : x |TX Lane is Enabled  : o |TX Lane is Enabled  : o |TX Lane is Enabled  : o |
|TX FIFO Overflow    : o |TX FIFO Overflow    : o |TX FIFO Overflow    : o |TX FIFO Overflow    : o |
|TX Send STOP        : o |TX Send STOP        : o |TX Send STOP        : o |TX Send STOP        : o |

|-- sFPDP RX            |-- sFPDP RX            |-- sFPDP RX            |-- sFPDP RX            |
|RX Lane is Enabled  : x |RX Lane is Enabled  : o |RX Lane is Enabled  : o |RX Lane is Enabled  : o |
|RX Link OK          : x |RX Link OK          : o |RX Link OK          : o |RX Link OK          : o |
|RX PCS Lane Locked  : x |RX PCS Lane Locked  : o |RX PCS Lane Locked  : o |RX PCS Lane Locked  : o |
|RX PCS Error        : o |RX PCS Error        : o |RX PCS Error        : o |RX PCS Error        : o |
|RX sFPDP Error      : o |RX sFPDP Error      : o |RX sFPDP Error      : o |RX sFPDP Error      : o |
|RX FIFO Overflow    : o |RX FIFO Overflow    : o |RX FIFO Overflow    : o |RX FIFO Overflow    : o |
|RX CRC Error        : o |RX CRC Error        : o |RX CRC Error        : o |RX CRC Error        : o |
|RX FIFO empty       : x |RX FIFO empty       : x |RX FIFO empty       : x |RX FIFO empty       : x |
|RX UDB FIFO Overflow: o |RX UDB FIFO Overflow: o |RX UDB FIFO Overflow: o |RX UDB FIFO Overflow: o |

Legend: o => false ; x => true
```

Example of Card and channel information usage

RAVEN-1 vs. RAVEN-3 vs. RAVEN-3_2

RAVEN-1 proposes serial communication channels fully compliant with VITA 17.1-2015 standard. RAVEN-1 is a modern and cost-effective interface solution to communicate with your legacy systems based on sFPDP protocol.

RAVEN-3 integrates the brand-new version of VITA 17.3-2018 sFPDP. **RAVEN-3_2** brings you high-effective serial communication protocol with no data rate limitation and up to date functionalities.

RAVEN-1, RAVEN-3 and RAVEN-3_2 share the same software interface. They allow you to have VITA 17.1 and VITA 17.3 protocols easily cohabiting in your system or to migrate quickly and with no risk from VITA 17.1 to VITA 17.3.

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